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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,482	03/12/2004	Akira Takahashi	OKI 414	6303

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EXAMINER	
ORTIZ, EDGARDO	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 04/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/798,482	TAKAHASHI, AKIRA	
	Examiner	Art Unit	
	Edgardo Ortiz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/12/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 1-2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the dummy gate made of non-doped polysilicon for polysilicon gate etching is disposed in area larger than the total area of the N type and P type polysilicon gates, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the

drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claim 1 is objected to because of the following informalities: Line 3 the claim reads "gates", the claim should read "*gate*". Line 5, the claims reads "disposed in area larger", it should read "disposed in *an* area larger". Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claims are unclear as to the claimed area for the dummy gate structure. It is unclear whether the dummy gate is formed in area larger than that of the N type polysilicon gate and P type polysilicon gate, or if the dummy gate occupies an area that is larger than that occupied by said N type polysilicon gate and P type polysilicon gate

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown et al. (U.S. Patent No. 6,703,269) in view of Morihara (Japanese Patent Publication 11-204506). As best the examiner is able to ascertain the claimed invention, with regard to Claim 1, Brown discloses a semiconductor device (column 1, lines 7-11) comprising:

an N-type (column 6, line 65-67 and column 7, line 1) polysilicon gate (70) and a P-type (column 7, line 1) polysilicon gate (71), wherein the gates are both disposed simultaneously over substrate (10), as disclosed in figures 4-7, which show the simultaneous formation through an etching process of the polysilicon gates (70, 71) over said substrate (10). See also, column 4, lines 66-67 and column 5, lines 1-5, which further disclose the implantation of impurities, P and N, on the gate structures to form said N-type polysilicon gate (70) and P-type polysilicon gate (71).

Brown fails to disclose the claimed dummy gate made of non-doped polysilicon for polysilicon gate etching is disposed in area larger than the total area of the N type and P type polysilicon gates. However, Morihara discloses (figures 4-7) a wafer formed with circuit pattern that includes gate electrode structures (8a) disposed between active regions (10a), a dummy gate (21a) made of non-doped polysilicon, since there is no dopant region defined in region C and it is

a well known practice in the semiconductor art to dope a gate structure during the formation of active regions, and the dummy gate (21a) is disposed in an area larger (figures 5-7) than the total area of the gate electrode structures (8a) formed between active regions (10a).

Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Brown to include the claimed dummy gate made of non-doped polysilicon for polysilicon gate etching is disposed in area larger than the total area of the N type and P type polysilicon gates, as suggested Morihara, in order to reduce dispersion in the processing dimension of a circuit pattern in a component formation area (paragraph 0022).

With regard to Claim 2, Brown discloses N-Type and P-type polysilicon gates (70, 71), the claimed impurities of boron and phosphor are commonly used materials in the semiconductor art to determine the conductivity, P or N, of conductive layers and thus would have been obvious to the ordinary artisan.

With regard to Claim 3, Brown discloses (column 5, lines 45-56 and figures 4-7) simultaneously gate-etching an N-type (column 6, line 65-67 and column 7, line 1) polysilicon gate (70) and a P-type (column 7, line 1) polysilicon gate (71).

Brown fails to disclose the claimed step of setting an etching area of a dummy gate made of

non-doped polysilicon for polysilicon gate etching larger than the total area of the N type polysilicon gate and the P type polysilicon gate to carry out said gate etching. However, Morihara discloses (figures 4-7) a wafer formed with circuit pattern that includes gate electrode structures (8a) disposed between active regions (10a), a dummy gate (21a) made of non-doped polysilicon, since the dummy gate (21a) is covered with an oxide layer (12) during the doping and formation of active regions (10a) (paragraph 0029), and wherein the dummy gate (21a) is disposed in an area larger than the total area of the gate electrode structures (8a) formed between active regions (10a) during the gate-etching process shown in figures 4-6.

Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Brown to include the claimed step of setting an etching area of a dummy gate made of non-doped polysilicon for polysilicon gate etching larger than the total area of the N type polysilicon gate and the P type polysilicon gate to carry out said gate etching, as suggested Morihara, in order to reduce dispersion in the processing dimension of a circuit pattern in a component formation area (paragraph 0022).

With regard to Claim 4, Brown discloses a gate etching process that is two-step process (column 6, lines 14-37) wherein a first step comprises a plasma-etch and a second step comprises an anisotropic-etch.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Brown et al. (U.S. Patent No. 6,703,269) in view of Morihara (Japanese Patent Publication 11-204506) and further in view

of Lee et al. (U.S. Patent No. 5,665,203). As best the examiner is able to ascertain the claimed invention, with regard to Claim 5, Brown discloses a two-stage etching process (column 6, lines 14-37) including a first stage using a mixed gas of HBr and O_2.

Brown fails to disclose the claimed second stage of etching using a mixed gas of HBr, O_2 and He. However, Lee discloses a semiconductor layer etching method that includes a gas mixture during an etching process, which uses a first stage atmosphere of Hbr, Cl_2 and He and a second stage atmosphere of HBr, O_2 and He (column 2, lines 39-41).

Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Brown to include the claimed second stage of etching using a mixed gas of HBr, O_2 and He, as suggested Lee, in order to obtain identical etch-behavior for n+ and p+ silicon (column 2, lines 17-19) and thus allow an improved etching process for polysilicon gate electrodes with n or p type dopants previously implanted (column 2, lines 4-7).

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edgardo Ortiz whose telephone number is 571-272-1735. The examiner can normally be reached on Monday-Friday (1st Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

E.O.
A.U. 2815
4/18/05

GEORGE ECKERT
PRIMARY EXAMINER